IN THE ABSTRACT

Please replace the Abstract with the Abstract attached herewith.

IN THE CLAIMS

Please amend claims 1-2, 4-11, and 13-14 as follows. All claims have been provided as a courtesy to the Examiner.

1. (Twice Amended) A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

first interface circuitry [configured] to receive from the system memory controller a first memory transaction in a first format; and

control logic coupled to the first interface circuitry and [configured] to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

2. (Twice Amended) The memory module controller of claim 1, further comprising:

second interface circuitry coupled to the control logic and [configured] to transmit the second memory transaction to at least one of the plurality of memory devices.

3. (Unchanged) The memory module controller of claim 1, wherein the first memory transaction includes time multiplexed address and command information.

4. (Twice Amended) The memory module controller of claim 3, wherein the first interface circuitry comprises:

request handling logic [configured] to separate the address and command information and to provide the separate address and command information to the control logic.

5. (Twice Amended) The memory module controller of claim 4, wherein the first memory transaction further includes time multiplexed data information, and wherein the request handling logic is [further configured] to separate the time multiplexed data information and to provide the separated time multiplexed data information to the control logic.

6. (Twice Amended) The memory module controller of claim 1, wherein the first interface circuitry comprises:

handshaking logic [configured] to provide a handshake signal to the system memory controller that indicates when the memory module controller is communicating data to the system memory controller.

7. (Twice Amended) The memory module controller of claim 1, wherein the first interface circuitry comprises:

data handling logic [configured] to receive data for the first memory transaction from the system memory controller and to reformat the data for the second memory transaction.

8. (Twice Amended) The memory module controller of claim 1, further comprising:

a write buffer coupled to the first interface circuitry and [configured] to store data sent with the first memory transaction.

9. (Twice Amended) The memory module controller of claim 8, further comprising:

an address storage unit coupled to the write buffer and the first interface circuitry and the address storage unit is [configured] to store addresses associated with the data stored in the write buffer.

10. (Twice Amended) The memory module controller of claim 1, further comprising:

a read buffer coupled to the control logic and [configured] to store data read from at least one of the plurality of memory devices.

11. (Twice Amended) The memory module controller of claim 1, further comprising:

a clock generator circuit coupled to the control logic and [configured] to receive a first clock signal from the system memory controller and to generate a second clock signal for the plurality of memory devices.

12. (Unchanged) A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

means for receiving from the system memory controller a first memory transaction in a first format; and

means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

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13. (Twice Amended) A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module comprising:

first interface circuitry [configured] to receive from the system memory controller a first memory transaction in a first format; and

control logic coupled to the first interface circuitry and [configured] to reformat the first memory transaction such that the plurality of memory devices perform the reformatted first memory transaction.

14. (Twice Amended) The memory module controller of claim 13, further comprising:

second interface circuitry coupled to the control logic and [configured] to receive from one of the plurality of memory devices a second memory transaction in a second

format, wherein the control logic [reformats] is to reformat the second memory transaction such that the system memory controller [performs] is to perform the reformatted second memory transaction.